REMARKS

Claims 1-11 are pending. The Examiner objects to claim 5 as being dependent upon a rejected base claims but indicates its allowability provided the Applicants rewrite the claim in independent form including all of the limitations of the base and intervening claims. The Examiner rejects claims 7-11 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,287,955 to Wang et al., in view of U.S. Pat. No. 6,376,048 to Takeishi. The Examiner rejects claims 1-5 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,051,508 to Takase et al., in view of Wang.

The Applicants amend claims 1-11 and add claims 12-15. Claims 1-15 remain in the application.

The Applicants add no new matter and request reconsideration.

Claim Objections

The Applicant sought clarification from the Examiner regarding claim 5. In a telephone message left August 26, 2002, the Examiner withdrew his allowance of claim 5 rejecting it together with claims 1-4 under § 103(a) as being unpatentable over Takase in view of Wang.

In a telephone conversation August 27, 2002, the Examiner stated that claim 6 is allowable provided the Applicants rewrite the claim in independent form including all of the limitations of the base and any intervening claims. The Applicants rewrite claim 6 in independent form to obviate the Examiner's objection. Claim 6 is in condition for allowance.

Claim Rejections Under § 103(a)

With regard to claims 7-11, the Examiner alleges Wang discloses all of the claimed subject matter except that Wang fails to specify organic and inorganic silicon oxide layers. The Examiner believes Takeishi provides the missing limitations in its Figures 5A-5C. The Applicants respectfully disagree for the reasons that follow.

Claim 7 recites *an organic silicon oxide layer of a low dielectric constant*. Wang fails to disclose an *organic silicon oxide* layer as the Examiner readily admits.

Contrary to the Examiner's allegations, however, Takeishi also fails to disclose an organic silicon oxide layer. Takeishi describes its second interlayer insulating film 20 as "made of the material similar to that of the organic insulating film shown in Figure 1A." Col. 8, 8:12. Takeishi discloses the materials forming its organic insulating film in Figure 1 A

"as...fluorocarbon (CF), fluorinated benzocyclobutene (PFCB manufactured by Dow Chemical Company), benzocyclobutene (BCB manufactured by Dow Chemical Company), fluorinated polyaryl ether (FLARE1.0 manufactured by Allied Signal Inc.), polyaryl ether (FLARE2.0 manufactured by Allied Signal Inc. or PAE manufactured by Schumacher Co.), parylene, polyimide, and fluorinated polyimide...." Col. 3, 26:34. None of these materials are *organic silicon oxide*s as required by claim 7. Thus, claims 7-11 and 14-15 are in condition for allowance.

With regard to claims 1-5, the Examiner alleges Takase shows all of the claimed subject matter except the low dielectric constant properties of the oxide layers and the trench formation detail. The Examiner believes Wang discloses the missing limitations. The Applicants disagree for the reasons that follow.

Claim 1 recites *forming a conductive region on a substrate.* Takase describes forming a first metal layer 22 on the surface of an interlayer dielectric 21. Takase further discloses "a silicon substrate in which elements are formed is [sic] exist under the interlayer dielectric 21." Col. 7, 25:27. Thus, the conductive region is not formed on the substrate as recited.

Claim 1 further recites *depositing an inorganic silicon oxide layer on the substrate* and *sequentially depositing an organic silicon oxide layer... on the inorganic silicon oxide layer.* The inorganic layer 13 is, therefore, formed below (and prior to the formation of) the organic layer 15 as shown in the Applicant's Figures 1-9. Takase, on the other hand, discloses in Figures 3A-3G, a device in which an inorganic SOG film 25 is formed after the formation of and above the organosiloxane film 23.

Claim 1 further recites *forming a partial trench ... in the organic silicon oxide layer.* Takase discloses etching the inorganic SOG film 25 and not the organic silicon oxide layer. Col. 7, 40:43.

Takase fails to disclose key limitations recited in claims 1-5. Therefore, claims 1-5 and 12-13 are in condition for allowance.

Conclusion

For the foregoing reasons, the Applicants request reconsideration and allowance of all remaining claims. The Applicants encourage the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Replace the paragraph beginning at page 1, line 18, with the following paragraph.

As interconnection density and integrated circuit density increase in semiconductor devices, the spacing between adjacent conductors decreases. As the spacing between adjacent conductors decreases, there is a corresponding increase in coupling capacitance (or mutual capacitance) between conductors. Adjacent conductors that exhibit a coupling or mutual capacitance form what is called a parasitic capacitor. In a typical integrated circuit device, parasitic capacitors are physically distributed over an integrated circuit and affect electrical operations therein. As the spacing between adjacent conductors decreases, the capacitance value of parasitic capacitors in an integrated circuit increases. Further, the topological widths of interconnections are decreased as circuit density is increased, causing an increase in the resistance of the interconnection.

IN THE CLAIMS

1. (Once amended) A method for fabricating a semiconductor device, comprising [the steps of]:

forming a conductive region on a substrate;

[sequentially] depositing an inorganic silicon oxide layer on [a] the substrate; [and]

sequentially depositing an organic silicon oxide layer of a low dielectric constant on the inorganic silicon oxide layer;

forming a partial trench with a predetermined depth in the organic silicon oxide layer [by patterning];

oxygenating an inner wall of the partial trench; and

forming a trench by etching the partial trench [with hydrofluoric acid (HF)].

2. (Once amended) The method of claim 1[, the method further] comprising [the steps of]:

depositing a conductive layer to fill the trench; and

removing a portion of the conductive layer stacked on a top surface of the organic

3. (Once amended) The method of claim 1[, the method further] comprising [the steps of]:

forming a photo resist pattern exposing a predetermined portion of a bottom of the trench after [the step of] forming the trench; and

forming a contact hole by etching the inorganic silicon oxide layer with the photo resist pattern.

4. (Once amended) The method of claim 1[,] wherein the oxygenation [is performed in an] includes ashing [step for] the photo resist pattern formed during the patterning step.

5. (Once amended) The method of claim 1[,] wherein the oxygenation is performed at a region having a thickness less than 1000 Å in an exposed region of the organic silicon oxide layer.

6. (Once amended) [The] A method [of claim 1, wherein] for fabricating a semiconductor device, comprising:

depositing an inorganic silicon oxide layer on a substrate;

sequentially depositing an organic silicon oxide layer of a low dielectric constant on the inorganic silicon oxide layer;

forming a partial trench with a predetermined depth in the organic silicon oxide layer;

oxygenating an inner wall of the partial trench; and

forming a trench by etching the partial trench with hydrofluoric acid (HF) [the HF wet etching is performed in] for about 5 seconds [by] using a buffered oxide etchant (BOE).

7. (Once amended) A semiconductor device, comprising:

a substrate having a conductive region formed thereon;

an inorganic silicon oxide layer formed on the substrate [and convering] to cover at least a portion of [a] the conductive region [formed thereon];

an organic silicon oxide layer of a low dielectric constant formed on the inorganic silicon oxide layer;

a conductive interconnection formed with a predetermined line width in a depth of the same or more as a thickness of] on the organic silicon oxide layer; and

a contact plug penetrating the inorganic silicon oxide layer in a predetermined [part] portion for electrically connecting [electrically] the conductive interconnection to the conductive region [of the substrate].

8. (Once amended) The semiconductor device of claim 7[,] wherein the contact plug and the conductive interconnection are simultaneously formed [in a manufacturing step].

9. (Once amended) The semiconductor device of claim 8[,] wherein the contact plug and the conductive interconnection are made of copper.

10. (Once amended) The semiconductor device of claim 7[,] wherein the organic silicon oxide layer is a silicon oxi-carbonate (SiOC) layer of silsesquioxane series containing carbon.

11. (Once amended) The semiconductor device of claim 10[,] wherein the organic silicon oxide layer is formed by chemical vapor deposition (CVD).

12. (New) The method of claim 1 wherein forming the partial trench includes patterning the partial trench.

13. (New) The method of claim 1 wherein forming a trench includes etching the partial trench with hydrofluoric acid (HF).

14. (New) The semiconductor device of claim 11 wherein the inorganic silicon oxide layer is made using a hydrogen silsesquioxane (HSSQ) precursor.

15. (New) The semiconductor device of claim 12 wherein the inorganic silicon oxide layer is formed by spin on glass (SOG) or chemical vapor deposition (CVD).